

ABSTRACT OF THE DISCLOSURE

Provided is an adder composed of  $(N+1)$  circuit stages in the case of  $2^N$  bits. In the case of  $N = 4$  (that is, 16 bits), provisional carriers that indicate the case where carry is produced from a low order bit and the case where no carry is produced therefrom are generated by conditional cells in a first circuit stage. In second to fourth circuit stages, the provisional carriers corresponding to higher seven bits other than the most significant bit are converted into provisional sums by converters in a circuit stage in which the provisional carriers are transferred. In addition, actual carry signals are selected from the provisional carriers corresponding to lower seven bits other than the least significant bit in a circuit stage in which the provisional carriers are transferred. In a fifth circuit stage, bit sums for each of the bits are generated and outputted.